FLARE
Open Deeply Programmable Network Node Architecture

FLARE Node Architecture

Control Plane
- x86 Processor
- Programmable

Data Plane
- Network Processor
- Programmable

Slice Architecture

Flare Board Rev.1.3 (New)

Network Processor PCIe Card
- 36-core TILE-Gx8036 Network Processor
- GbE: 8 ports and 10GbE SFP+: 2 ports
- Up to 16GB memory
- PCI Express 2.0 : x8

To use Manycore Network Processor: TILE-Gx72

Acknowledgment: This research is supported by MIC SCOPE
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**LTE Softwarization on FLARE**

- EPC signaling and HSS implemented by dockers in c-plane of FLARE slice
- User data processing implemented by Click in d-plane of FLARE slice
- Southbound API provides SDN messages to create/remove/update GTP-U tunnel

### Slicing EPC on FLARE

- **Control Plane**
  - eNB
  - VLAN
  - FLARE Switch
    - FLARE Slice 1 (c-plane)
    - FLARE Slice 2 (c-plane)
    - PCIe
    - Southbound API

- **Data Plane**
  - SP-GW (d-plane)
  - Slicer slice

- **Signaling**
  - HSS
  - MME

### Slicing eNB on FLARE

- **FLARE Server**
  - FLARE Slice 1
    - docker
    - eNB
  - FLARE Slice 2
    - docker
    - eNB

- **Passthrough**
  - USB
  - vNIC

- **Open vSwitch**
  - VLAN

- **Universal Soft Radio Peripheral (USRP)**
  - USRP B210

### Demo Setup for LTE Softwarization in FLARE Slice

- **FLARE Mobile**
- **FLARE eNB**
- **FLARE EPC**

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